REMARKS

Reconsideration of the application is requested.

Applicants appreciatively acknowledge the Examiner's confirmation of receipt of applicant's claim for priority under 35 U.S.C. § 119(a)-(d).

Claims 1-10 remain in the application.

In item 3 on page 2 of the above-identified Office Action, claims 1, 3-6, and 9 have been rejected as being fully anticipated by Fang (U.S. Patent No. 6,316,293) under 35 U.S.C. § 102.

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and, therefore, the claims have not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*:

> providing a substrate divided into a high-voltage region, a memory region and a logic region;

forming a first insulating layer on the substrate in the high-voltage region, the memory region and the logic region;

removing the first insulating layer in the memory region;

forming a second insulating layer in **the high-voltage region, the memory region and the logic region.**

The second insulating layer is seen in Figs. 3B, 4B, 5B, and 5C of the instant application. Looking to Fig. 3B in conjunction with Fig. 3A, three distinct regions can be seen. The three regions are labeled HVB, NSB, and LB, designating a high-voltage region, a nonvolatile memory region, and a logic region, respectively. As is shown in Fig. 3B, and explained on page 9, lines 13-14 of the instant application, the second insulating layer (tunnel oxide layer) 3 is formed **over all three regions**, HVB, NSB, and LB. Because, as recited in claim 1, a first insulating layer 2 has been formed on the HVB, and the LB regions, the second insulating layer is necessarily formed **on** the first insulating layer 2. As is also explained on page 9, lines 18-24 of the instant application, the tunnel oxide layer 3, together with the first insulating area 2, forms a high-voltage oxide layer 4. High-voltage oxide layer 4 is an important element of the present invention, especially in the high-voltage region.

The Fang reference discloses a method of forming NAND-type flash memory devices. The disclosed method forms a core memory cell 105 and periphery transistors (both high voltage 118 and low voltage 116), as seen in Fig. 5c and described in col. 7, lines 38-43 of Fang. Fang discloses a tunnel oxide layer 119 grown only in a single area 114, which is itself located in the single core region 105. This structure is fully explained in col. 6, lines 6-32 and one looking at Fig. 5d of Fang can easily see that the tunnel oxide layer is located only between the layers 108, which acts as a barrier to contain the tunnel oxide layer 119.

Clearly, Fang does not disclose forming a tunnel oxide layer over a high-voltage region, a nonvolatile memory region, and a logic region as recited in claim 1 of the instant application. Nor does Fang disclose the formation of the tunnel oxide layer on a first insulation layer in the high-voltage region and the logic region, as does claim 1 of the instant application. A comparison of Fig. 5d of Fang and Fig. 3B of the instant application quickly shows this difference.

It is accordingly believed to be clear that the Fang reference does not show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the

art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

In item 12 on page 5 of the above-identified Office Action, dependent claim 2 has been rejected as being obvious over Fang in view of Babayan (U.S. Pat. No. 6,194,036) under 35 U.S.C. § 103.

In item 14 on page 6 of the above-identified Office Action, dependent claims 7 & 8 have been rejected as being obvious over Fang in view of the Ghandhi publication under 35 U.S.C. § 103(a).

In item 17 on page 6 of the above-identified Office Action, dependent claim 10 has been rejected as being obvious over Fang in view of Wu (U.S. Pat. No. 6,261,964) under 35 U.S.C. § 103(a).

As stated in the preceding paragraphs, it is believed that Fang does not disclose the limitations contained within independent claim 1. Because claims 2, 7, 8, and 10 are dependent on claim 1, they too are believed to be allowable. Considering the deficiencies of the Fang reference, it is believed not to be necessary at this stage to address the secondary references applied in the rejection of claims 2, 7,

8, and 10 and whether or not there is sufficient suggestion or motivation with a reasonable expectation of success for modifying or combining the references as required by MPEP § 2143.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

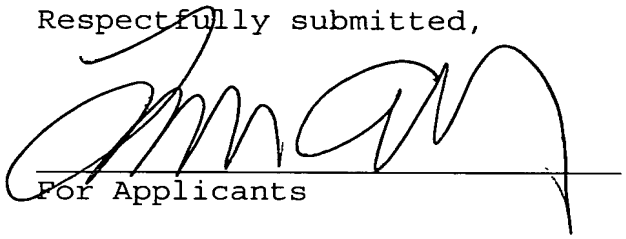
In view of the foregoing, reconsideration and allowance of claims 1-10 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

Petition for extension is herewith made. The extension fee for response within a period of 2 month pursuant to Section 1.136(a) in the amount of $420.00 in accordance with Section 1.17 is enclosed herewith.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,



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